

Name of Scholar : MD EJAZ ASLAM LODHI
Name of Supervisor : Prof. Abdul Quaiyum Ansari
Name of Department : Department of Electrical Engineering
Topic of Research : Design and Simulation of High Performance Power Semiconductor Devices.

Findings

Semiconductor-based power-oriented devices are found in many cutting-edge classified sectors, such as mobile phones with heavy usage, radio frequency measurements, cars, high-speed trains, strategically positioned satellites, and more. These applications cover power consumption levels ranging from watts to megawatts (MW) or kilowatts (KW). In the world of device research, Si Power MOSFET is acknowledged as a crucial device of great significance and interest. Numerous factors influence the design of power MOSFETs. Power device researchers' main goals in the context of switching devices are to minimize both switching and conduction losses. Numerous cutting-edge power MOSFETs are the product of ongoing research on power semiconductor MOSFETs. According to these power device studies, keeping the source and drain terminals of older power devices in a horizontal alignment that relied on lateral orientation led to noticeably higher specific device on-resistance, usually because of the large working area (active) of the electronic device. The aforementioned problem was lessened by a reading on the current advanced vertical power MOSFET.

Additionally, prior studies on silicon and other material power devices have shown that a paired gate performs better than a solo gate, reducing the uncertainty of V_{th} brought on by changes in channel dimension. However, the power structure encountered sudden variations in the electric field between the dualism gates, whereas the typical solo trench gate MOSFET experiences considerable electric field crowding at the gated-trench polysilicon gate bends, which leads to a low breakdown voltage. In terms of configuration, vertical trench gate power MOSFETs have many advantages over lateral power MOSFETs because the vertical design avoids the accumulation zone, which reduces the related resistance. Conversely, employing the double charge balance technique approach significantly improves device performance, reduces the gate-to-drain terminal capacitive (C_{gd}) coupling, and minimizes the overall gate charge demand. Due to their remarkable gate control and high ON-current, triple-gate planar devices have recently added a new dimension to current research.

The present works (presented as chapter wise in this Ph.D. work) addresses all issues that governs the power MOSFET, by introducing multi gate engineering, Super Junction/Split Gate technology and simultaneously using different high mobility channel materials like SiGe and GeSn, comparing with conventional Si based power MOSFET, enhancing the CMOS performance.

In the first work, the problem of lower channel mobility in Si is addressed by high mobility channel materials like SiGe and GeSn, over Si, used in selective buried triple gate trench vertical power trench MOSFET. This work aims to enhance the device's p-body (channel) electron mobility, which is an essential component of all MOSFETs. The proposed device consists of a single vertical polysilicon trench in the drain (drift) area and two selected buried (facing each other) lateral gates. The proposed device, which uses GeSn material and has orthogonally oriented gates for the first time, achieves increased electron mobility and transconductance. In the projected power MOSFET industry, the proposed triple gate's unique design achieves a channel structure mobility of up to $880 \text{ cm}^2/\text{V}\cdot\text{s}$. The results show that our suggested device's improved power MOSFET parameters achieve a super tiny specific device ON-resistance value of $0.31 \text{ m}\Omega\cdot\text{cm}^2$, which enhances Baliga's FOM1 by 411.61% and FOM2 by 98.704%. This feature makes it close to the perfect switch, supporting cutting-edge speed and

switching devices, guaranteeing compatibility with a variety of high mobility channel (p-body) materials, and successfully placing it for future CMOS usage.

Further work presents a novel vertical power MOSFET super junction and split gate-based power structure, which employs a double-charge balanced method, projected and considered for the earliest time. The double-charge balanced method is implemented by dividing the trench polysilicon gate and transforming the n-drift region into a series of charged drift balanced p/n pillars. This approach notably enhances device performance and minimizes the overall gate charge requirement, along with reducing the gate-to-drain terminal capacitive (C_{gd}) coupling. The projected Si device demonstrates a gate charge (Q_{gd}) of 0.94 pico-coulomb, indicating a 33.6% enhancement in breakdown voltage. Additionally, improvements of 74.1%, along with 99.29%, are observed in Baliga's Figure of Merits (FOM1 and FOM2), along with a 91.62% increase in C_{gd} , achieved at 1.2 μm thick epilayer (Si material). These results highpoint the superior characteristics of the projected vertical structure compared to the current state-of-the-art, utilizing dual distinct charge balancing techniques with no compromising on the gate control.

Further work proposes an innovative vertical trench added epilayer with p+ shielded accumulation mode trench MOSFET device. The application of ATLAS software 2-D simulation utilising various models has yielded significant results regarding switching performance and figure of merit when associated to the traditional accumulation mode MOSFET. The extracted charge is 38.2 pC associated with the gate terminal to drain (Q_{gd}), with a figure of merit (FOM) of about 31.71 $\text{m}\Omega\cdot\text{nC}$, at active cell pitch of 3 μm , in the presented new-fangled device. Therefore, the projected device validates superior show associated to the previous accumulation mode trench MOSFET in minimizing the overall gate terminal charge required and reducing gate terminal-to-drain capacitive (C_{gd}) coupling, while maintaining the integrity of the channel regulated mechanism using gate terminal.

The modeling of a charge-sensitive super junction unique vertical trench (Si material) epilayer with p+ shielded accumulation mode MOSFET device with a Super Junction in the drift region is shown in the additional study. By utilizing ATLAS 2-D numerical simulation, which combines many physics models, this modifies the tradeoff connection between RON and Breakdown Voltage (BV), exceeding the traditional silicon limit line. By adding a p+ barrier at the end of the trench, the suggested device has well-isolated gate and drain regions. Furthermore, the super junction lower drift layer is still unable to access the device channel. When compared to the conventional accumulation mode trench MOSFET, the suggested device shows a significant improvement in acceptable breakdown voltage, speed, switching performance, and figure of merit. The device has a figure of merit (FOM) of approximately 22.65 $\text{m}\Omega\cdot\text{nC}$, a breakdown voltage of around 31.0 V, a gate-to-drain charge value of 23.6 pC, and a cell pitch of 3 μm . The simulation research that follows shows a significant decrease in gate-to-drain device capacitance. Both Baliga's Figure of Merit (FOMs) have significantly improved as a result of the addition of a vertical n-added Epilayer and a horizontal p+ strip, as well as the use of Super Junction technology in the drift region.

Lastly, our next work examines the different properties that govern a power MOSFET, specifically focusing on a novel and unique vertical triple gate selective buried trench power MOSFET. The latest innovation is a Triple Gate Power MOSFET (TGSBTPMOS), which consists of a MOSFET with two lateral selective buried gates and one vertical trench gate facing the drift area. In the voltage range of 78.8 V, the combination of three gates results in a significantly higher device ON-state current and a very low ON resistance of about 0.38 $\text{m}\Omega\cdot\text{cm}^2$. Multiple inversion layers are incorporated into the proposed device to enable an increase in on-current and channel width. When compared to traditional power MOSFETs, this improvement results in better static state and switching performance. The suggested device shows improvements of 4.86 orders of magnitude in FOM1, 68.85% in $R_{on,sp}$, 94.54% in Q_{gd} , and 98.34% in FOM2. When compared to the reported power Si MOSFET structure, the suggested device shows competitive performance and provides an improvement over the current state of the art.

This work summarizes the introduction of many novel power devices, for the first time. By introducing Triple gate power MOSFET (orthogonally oriented novel selective buried trench triple gate), double gate vertical power trench MOSFET using Super Junction/Split Gate technology, and

concurrently using different elevated mobility channel materials like SiGe and GeSn, in comparison with conventional Si based power MOSFET, this work addresses all issues related to power MOSFET administration. The carrier balanced super junction along with split polysilicon gate vertical trench power MOSFET (SJSGTPMOS) structure, n mode vertical trench added Si epilayer with p⁺ (as shield resist) power MOSFET, vertical trench epilayer with p⁺ shielded accumulation mode MOSFET device, multiple inversion layer selective buried novel triple gate vertical trench power MOSFET (TGSBTPMOS), and materials like Si/SiGe/GeSn, which is utilized in orthogonally oriented with selective buried novel triple gate vertical power MOSFET. When compared to traditional power MOSFETs, the suggested devices show many-fold improvements in BV, Ion, FOM1, Ron.sp, Qgd, and FOM2. When compared to the stated power MOSFET structure, the suggested device shows competitive performance and is an improvement above the current state-of-the-art.